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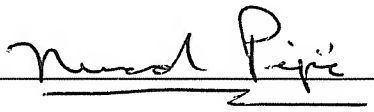
Signature: 

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Martinez et al.	:	**Examiner:** A. Riad
Ser. No.: 10/781,477	:	**Art Unit:** 2113
Filed: Feb. 17, 2004	:	**HP PD No.** 200314423-1
For: System and Method for Reboot Reporting	:	**Confirmation No.** 3109

Appeal Brief

Mail Stop Appeal Brief-Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

The following appeal brief is submitted pursuant to the notice of appeal filed May 14, 2007 and the Notice of Panel Decision from Pre-Appeal Brief Review mailed on Aug. 1, 2007.

REAL PARTY IN INTEREST

The real party in interest is HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P. located at 20555 SH 249, Houston, Texas 77070.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-30 are pending in this appeal. All claims stand rejected under § 102(e) in view of U.S. Pat. No. 6,732,298 to Murthy et al. (hereinafter "Murthy").

STATUS OF AMENDMENTS

All amendments to the claims have been entered on the record and none are outstanding.

SUMMARY OF THE CLAIMED SUBJECT MATTER[1]

Independent claim 1 is directed to a method of "reboot reporting." Figure 2 is representative of the claimed invention and reproduced below:

[1] This summary of the claimed subject matter is not intended to limit the scope of the claims to the portions of the specification and drawings cited herein. Citations to the specification and drawings are made solely for the purpose of satisfying 37 C.F.R. § 41.37.

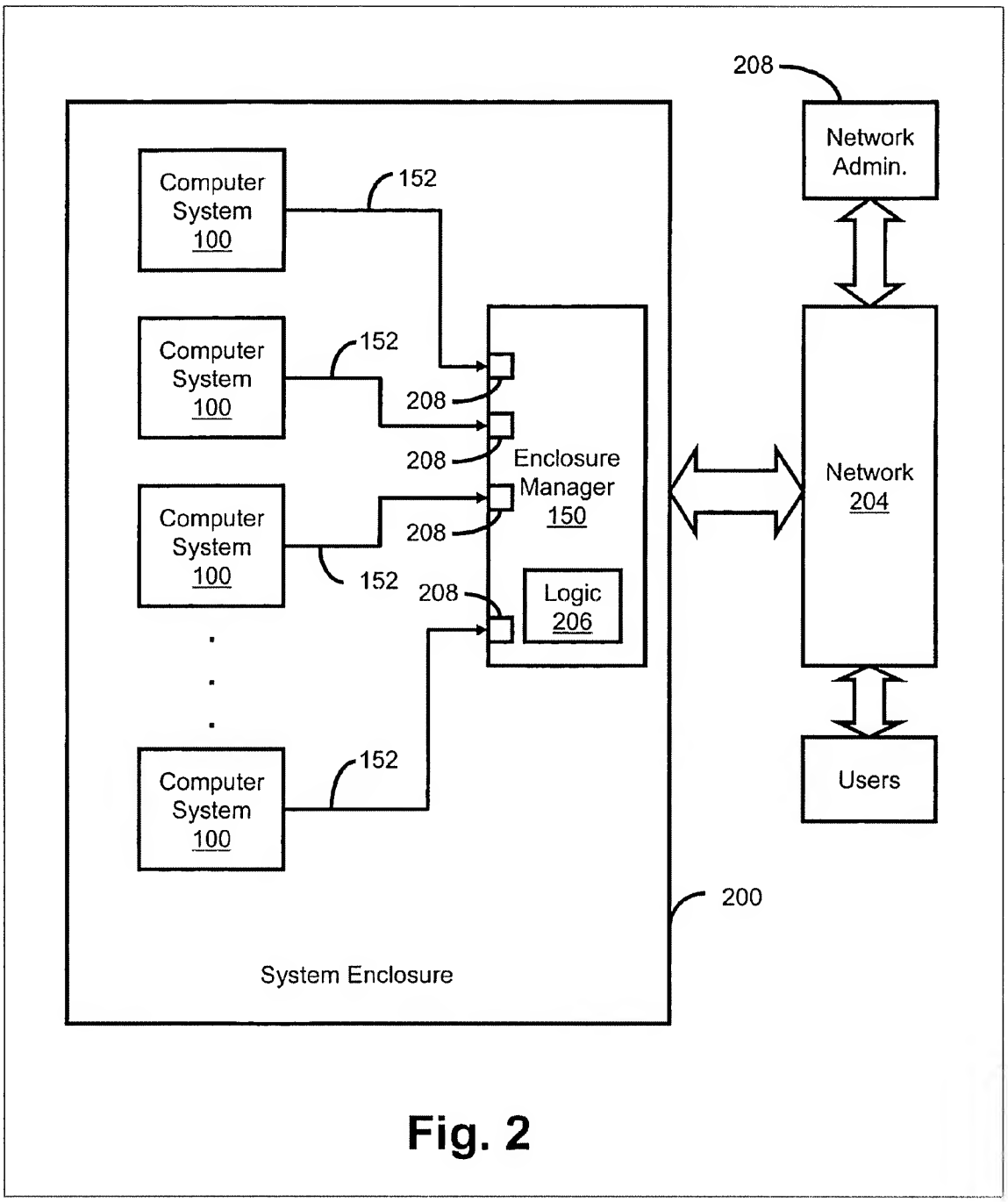


Fig. 2

As shown in Fig. 2, a plurality of input lines 152 associated with a plurality of computer systems 100 having a plurality of processors are read by an enclosure manager 150. At least one non-maskable interrupt signal is generated within computer systems 100 and output to a processor of the computer systems 100 and, on line 152, to an enclosure

manager 150 associated with the plurality of computer systems 100. An indication that at least one computer system 100 has a fault condition is then generated.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-30 are patentable under 35 U.S.C. § 102(e) over Murthy. Claims 2-4, 6-18, and 20-30 stand or fall with independent claim 1 and claim 19 stands or falls with dependent claim 5.

ARGUMENT

Claim 1 describes a method of reboot reporting comprising:

> reading a plurality of input lines associated with a plurality of computer systems having a plurality of processors;
>
> generating at least one non-maskable interrupt signal;
>
> outputting the non-maskable interrupt signal to a processor of the plurality of computer systems;
>
> outputting the non-maskable interrupt signal to a manager associated with the plurality of computer systems; and
>
> generating an indication that at least one computer system has a fault condition.

The Final Rejection rejects claim 1 as being unpatentable under 35 U.S.C. § 102(e) in view of Murthy.

It is well-known that under § 102, anticipation requires **each and every claim element to be found in a single reference**. Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631 (Fed. Cir. 1987). If a claim element is missing from a relied upon reference, a rejection under § 102 cannot be sustained.

In order for a rejection under § 102 to be sustained, it is clear that the relied-upon Murthy reference must disclose a non-maskable interrupt. It is respectfully submitted that Murthy **clearly does not** disclose a non-maskable interrupt and, therefore, the

rejection under § 102 cannot be sustained. In particular, the Abstract of Murthy unequivocally states that non-maskable interrupts are not used:

> "A system and method is disclosed for debugging of a hardware board that includes a processor with only a ***single level of interrupts*** that are either all enabled or all disabled. ***The processor does not implement nonmaskable interrupts.***" (Emphasis added).

Nevertheless, the Final Rejection on pg. 3 attempts to sustain the § 102 rejection by relying on Murthy's Summary of the Invention at col. 2, lines 59-66, which states:

> "The problems noted above are solved in large part by a single level interrupt processor on the array controller board that contains a critical failure input line that permits implementation of a nonmaskable pseudo-interrupt for debugging of the array controller. The nonmaskable pseudo-interrupt informs the processor of a debug request even when all device interrupts in the processor are disabled and the array controller board is inoperative."

In particular, it appears that the Final Rejection is relying on the disclosure that an "array controller board that contains a critical failure input line that permits implementation of a ***nonmaskable pseudo-interrupt*** for debugging of the array controller" (emphasis added).

In ordinary English usage, the word "pseudo" means "false or counterfeit; fake." (See, "pseudo." *The American Heritage® Dictionary of the English Language*, 4th ed. Boston: Houghton Mifflin, 2000. www.bartleby.com/61/. [accessed May 2, 2007]. Because the processor of Murthy ***"does not implement nonmaskable interrupts"*** (Abstract), Murthy adapts a different signal -- a critical failure input line -- and refers to it as a nonmaskable psuedo (*i.e.,* false or counterfeit; fake) interrupt. Due to the acknowledged lack of non-maskable interrupts, Murthy takes a different approach by relying on a critical failure input line which is identified as a machine check exception signal 61. Hence, the relied-upon Summary of the Invention is consistent with the Abstract in that non-maskable interrupts are **expressly not implemented by Murthy**.

Therefore, it is respectfully submitted that the ***§ 102 rejection*** of the independent claims cannot be sustained because Murthy expressly discloses that its processor **does *not implement nonmaskable interrupts.***

Dependent claim 5 requires "counting the number of times the non-maskable interrupt signal is generated." The Final Rejection asserts on pg. 5 that this limitation is met by the following Murthy disclosure:

> "As shown in FIG. 2, various interrupts (int 0, int 1, int 2 . . .) are generated by the devices given in FIG. 1 and FIG. 2 and are handled by processor 58."

In particular, the Final Rejection states that the "Examiner considers the listing of int0, int1, int2, as counting interrupts" (p. 16). The listing in the cited Murthy disclosure is clearly a reference to the structure shown in Figure 2, which has been reproduced below with arrows annotating the structure, and is not a process step of "counting the number of times the non-maskable interrupt signal is generated."

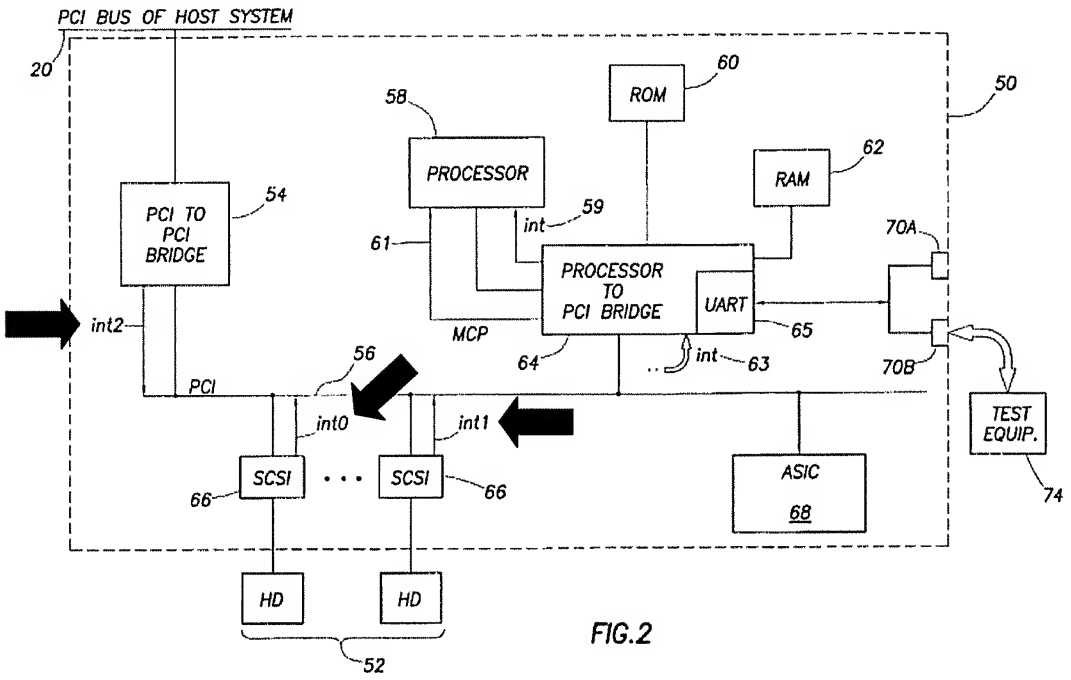


FIG.2

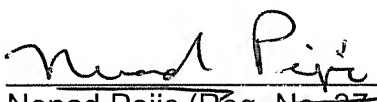
Figure 2 of Murthy (Annotated with Arrows)

In other words, the listing of "int0," "int1," and "int2" are reference labels to separate system components shown in Fig. 2 of Murthy, not to a process step counting the number of times a non-maskable interrupt signal is generated, as claimed. Hence, it is respectfully submitted that the relied upon disclosure does not teach or suggest the "counting . . ." limitation of dependent claim 5.

Conclusion

For the reasons advanced above, it is respectfully submitted that the §102(e) rejection of the independent claims cannot be sustained because Murthy expressly states that its processor does not implement non-maskable interrupts. It is also respectfully submitted that dependent claims 5 and 19 are patentable on their own merits because the relied-upon description listing the reference labels used in drawing Figure 2 of Murthy does not teach or disclose a process step of "counting the number of times the non-maskable interrupt signal is generated." Reversal of the § 102(e) rejections in this appeal is respectfully requested.

Respectfully submitted,



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APPENDIX

The Claims Under Appeal

1. A method of reboot reporting comprising:

reading a plurality of input lines associated with a plurality of computer systems having a plurality of processors;

generating at least one non-maskable interrupt signal;

outputting the non-maskable interrupt signal to a processor of the plurality of computer systems;

outputting the non-maskable interrupt signal to a manager associated with the plurality of computer systems; and

generating an indication that at least one computer system has a fault condition.

2. The method of claim 1 further comprising associating the non-maskable interrupt signal with at least one computer system of the plurality of computer systems.

3. The method of claim 2 further comprising generating a notice identifying the at least one computer system.

4. The method of claim 3 further comprising redistributing the processing load from the at least one computer system to the remaining plurality of computer systems.

5. The method of claim 1 further comprising counting the number of times the non-maskable interrupt signal is generated.

6. A system for reboot reporting comprising:

a plurality of computer systems having at least one processor and at least one non-maskable interrupt output;

a manager system in circuit communication with the plurality of computer systems and comprising at least one non-maskable interrupt input associated with the plurality of computer systems.

7. The system of claim 6 wherein the plurality of computer systems comprises a plurality of non-maskable interrupt outputs and the manager system comprises a plurality of non-maskable interrupt inputs.

8. The system of claim 7 wherein the non-maskable interrupt outputs of the plurality of computer systems are in circuit communication with the plurality of non-maskable inputs of the manager system.

9. The system of claim 6 wherein the plurality of computer systems comprises at least one computer system having a processor, a first bridge circuit and a second bridge circuit and wherein the second bridge circuit comprising a non-maskable interrupt signal output in circuit communication with the processor.

10. The system of claim 9 wherein the non-maskable interrupt output of the second bridge is in circuit communication with the manager system.

11. The system of claim 6 further comprising logic for reading at least one non-maskable interrupt input associated with the plurality of computer systems.

12. The system of claim 11 further comprising logic for generating an indication that at least one computer system has a fault condition based on the presence of a non-maskable interrupt signal present on the at least one non-maskable interrupt input.

13. A system for reboot reporting comprising:

a plurality of computers comprising at least one means for processing;

means for managing the plurality of computers; and

means for outputting a non-maskable interrupt signal indicating a fault condition associated with at least one of the plurality of computers to the means for managing and to the at least one means for processing.

14. The system of claim 13 further comprising means for detecting the non-maskable interrupt signal indicating a fault condition associated with at least one of the plurality of computers and generating a detection signal in response thereto.

15. The system of claim 13 further comprising means for generating at least one non-maskable interrupt signal.

16. The system of claim 13 further comprising means for generating an indication that at least one computer has a fault condition.

17. The system of claim 13 further comprising means for associating the non-maskable interrupt signal with at least one computer of the plurality of computers.

18. The system of claim 17 further comprising means for redistributing the processing load from the at least one computer to the remaining plurality of computers.

19. The method of claim 13 further comprising means for counting the number of times the non-maskable interrupt signal is generated.

20. A computer system comprising:

a processor;

a memory;

at least one bridge circuit in circuit communication with the processor;

a non-maskable interrupt signal circuit in circuit communication with the processor and at least one other computer system.

21. The system of claim 21 wherein the at least one other computer system comprises an enclosure manager.

22. A system comprising:

an enclosure having a plurality of individual computer systems and a manager computer system;

wherein at least one of the plurality of computer systems comprises a processor and a non-maskable interrupt signal circuit, the non-maskable interrupt signal circuit in communication with the processor and the manager computer system, the non-maskable interrupt signal circuit comprising a bridge circuit and a non-maskable interrupt signal path to the processor and the manager computer system.

23. The system of claim 22 wherein the manager computer system comprises a non-maskable interrupt signal input.

24. The system of claim 23 wherein the manager computer system comprises logic for reading a state of the non-maskable interrupt signal input.

25. The system of claim 24 wherein the manager computer system comprises logic for generating a notice based on the state of the of the read non-maskable interrupt signal input.

26. A system comprising:

means for housing a plurality of digital devices;

means for managing the plurality of digital devices, said means for managing comprising a location within said means for housing;

means for receiving and processing executable instructions, said means for receiving and processing comprising a location within said means for housing;

means for generating a non-maskable interrupt signal; and

means for communicating the non-maskable interrupt signal to the means for receiving and processing and to the means for managing.

27. The system of claim 26 wherein the means for communicating the non-maskable interrupt signal to the means for receiving and processing and to the means for managing comprising a non-maskable interrupt signal pathway.

28. The system of claim 26 wherein the means for managing the plurality of digital devices comprises means for reading the state of the means for communicating and means for generating a notice based on the state of the means for communicating.

29. The system of claim 26 wherein the means for managing the plurality of digital devices comprises means for re-distributing a processing distribution among the plurality of digital devices.

30. The system of claim 26 wherein the means for generating a non-maskable interrupt signal comprises a bridge circuit associated with the means for receiving and processing.

EVIDENCE APPENDIX

(NONE)

RELATED PROCEEDINGS APPENDIX

(NONE)